A 5.3-9.3 fJ/Conversion-Step 4-32 MS/s 10 bit Asynchronous SAR ADC with Optimized DAC Timing Strategy in 0.13 µm CMOS

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Abstract. In this paper, a low power SAR Analog to Digital Converter (ADC) with a resolution of 10 bits and a sampling rate of 4 to 32 MS/s is proposed. It utilizes an asynchronous process with an optimized D/A timing strategy to increase its sampling frequency. This ADC is simulated in a 130-nm CMOS technology with two power supplies of 0.6 V and 1.2 V. It achieves an ENOB greater than 9.3 bits for its full sampling-rate range (4 to 32 MS/s) with an FOM = 5.3 to 9.3 fJ/conv.-step.

Keywords: Analog to digital converter; asynchronous process; power efficiency; asynchronous clock generator circuit; low power designs.

1. Introduction

Some of the applications of ADCs with a medium resolution (8 to 10 bits) and medium frequencies (a few tens to hundreds of MS/s) include applications in wireless networks and digital TV [1]. Pipeline ADCs have been one of the conventional candidates for such applications. However, this ADC architecture needs some operational amplifiers with high bandwidths and gains to have a good linearity and therefore, requires high power consumption [1]. For this reason, SAR ADCs have received more attention in recent years. This ADC not only needs small area and consumes low power, but also can achieve up to 400MS/s in single channel SAR [2]. In this structure, thanks to technology scaling, the problem of long conversion time have been alleviated. Moreover, since the output bits are serially produced, with increasing the circuits resolution, sampling rate is then decreased.

Recently, different techniques have been also reported to increase the speed of SAR ADCs such as multi-bit/step [3] and time interleaving [4]-[5]. Using asynchronous process to realize internal comparisons of the converter is another appropriate method that has been presented [6]-[7] to speed up the conversion rate. In [6], it has been proved that the maximum asynchronous conversion time is half of that in its synchronous counterpart. This method also removes the need for some internal clock generator circuit and hence it saves some area and power. In this paper, a new approach to asynchronous processing is presented that, compared to the conventional method; it can further increase the speed of the converter with high power efficiency. The proposed asynchronous process is applied to a 10-bit 4-32 MS/s SAR ADC.

The paper is organized as follows. In Section 2, the conventional asynchronous process of the converter and also its challenges are discussed. The proposed asynchronous process, its circuit level implementation, and its power and area considerations are presented in Section 3. Also in this section, the effectiveness of the target asynchronous process method compared to its conventional counterpart is discussed. A 10-bit SAR ADC with a sampling rate of 4MS/s to 32MS/s that utilizes the proposed asynchronous process is presented in Section 4. In this section, the converter structure is benefited from the monotonic capacitor switching procedure that has suitable power efficiency due to the reduction in the switching energy [1]. In Section 5, the effectiveness of the proposed asynchronous process technique is shown using extensive simulation results in 130 nm digital CMOS process.

Manuscript received May 30, 2014; revised August 8, 2014; accepted August 16, 2014.

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2. Conventional Asynchronous SAR ADC

A conventional SAR ADC architecture is shown in Fig. 1-a. The building blocks of a SAR ADC are comparator, digital to analog converter, and digital state machine that is also known as SAR logic. Binary search algorithm is realized by successively comparing the input voltage with multiplications of $V_{REF}/2^n$ (where V_{REF} is the ADC reference voltage and n is the ADC resolution).

In a conventional synchronous process, the conversion time is divided into two phases: sampling phase and conversion phase, as shown in Fig. 1-b. According to this figure, the conversion phase itself consists of some clock cycles to generate MSB to LSB bits. In order to make n bits in a synchronous process with a sampling rate of f_S, an internal clock frequency of $f_S \times (n+1)$ is required. In case of low speed and low resolution, producing internal clock is less challenging, whereas producing this clock and applying it to the chip becomes critical in high speed and high resolution applications [6]. For example, for a sampling rate of 400 MS/s and a resolution of 6 bits, an internal clock frequency of 2.8 GHz is needed. In a synchronous process, producing such internal clock and distributing it among the converter devices requires high power consumption.

Moreover, each clock cycle is designed according to the maximum comparison time, maximum settling time of the digital to analog converter (DAC), and a time margin required for dealing with the jitter [6]. Therefore, both speed and power consumption is deteriorated in a high-speed synchronous process [6].

In order to resolve the problems associated with the synchronous process, asynchronous process is used [6]. In this process, an external clock associated with the sampling

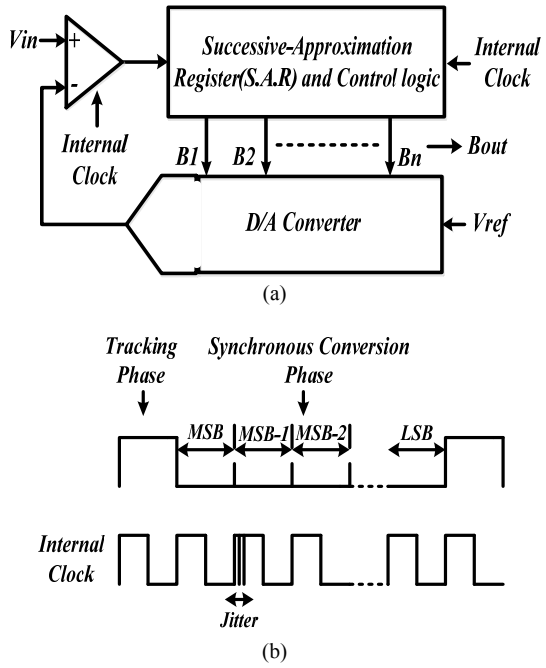


Fig. 1. (a) Architecture of the conventional SAR ADC. (b) Synchronous processing with equally devided bit comparison time.

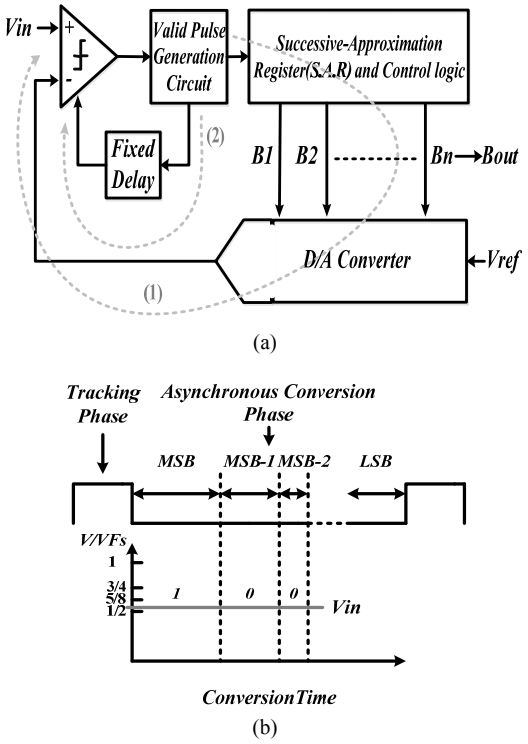


Fig. 2. (a) Architecture of the conventional asynchronous SAR ADC. (b) Conventional asynchronous process timings.

rate of the converter is applied to the converter and the component clocks are produced internally. The dedicated time to each bit from MSB to LSB is based on the time required for the comparator to decide [6].

The architecture of the SAR ADC based on the asynchronous process and the corresponding clock phases are shown in Fig. 2. Here, once the comparator's output is ready, a control signal, named as Valid, is produced by the comparator to confirm that the next clock cycle may start (path 2 in Fig. 2(a)). However, the next clock cycle cannot start unless the SAR logic and the DAC generate the next comparison voltage at the input of the comparator (path 1 in Fig. 2(a)). Thus, a *fixed delay* must be added to this valid signal in path 2 before going to the comparator. It is shown in [6] that, in average, less time are required for the total conversion phase using the asynchronous process. Note that, in a conventional asynchronous process, this fixed delay is determined based on the SAR logic delay and worst-case delay of the DAC settling time (i.e., when the MSB capacitor must be charged).

As explained in [7], the pulse width dedicated to each DAC capacitors (and, hence, the ADC clock frequency) strongly depends on the DAC settling time. Therefore, to reduce the total DAC settling time, two design options for the DAC switching can be used: 1) utilizing the same size switches with low equivalent resistance in the DAC for all bits, such that the DAC R-C time constant (τ) is small in order to have a fast settling response, and 2) equalizing the settling time from MSB to LSB with scaled switches [7]. If the settling accuracy is designed to be the same for all bits, the DAC settling time decreases from MSBs to LSBs. Thus, for LSB capacitors, since the step voltage is small, the pulse width dedicated for its settling can be reduced to achieve higher speed.

3. The Proposed Asynchronous SAR ADC

3.1. Architecture

As mentioned in the previous section, in a conventional asynchronous SAR ADC, the '*fixed delay*' is determined based on the worst-case delay required for the DAC settling time. However, the settling time for each of the D/A array capacitors are different. The switching of the DAC array reduces the settling time. Thus, the delay in path 2(Fig. 2-a) can be reduced when moving from MSB to LSB capacitors, and hence, the total A/D conversion time can be reduced.

The schematic of the proposed SAR structure in its asynchronous conversion phase (the cycle associated with generating the (MSB-1) to the LSB bits), and the target asynchronous process approach are represented in Figs. 3(a) and 3(b), respectively. As can be seen in the figures, τ_i and k_i are the time constant and accuracy of DAC settling for the DAC capacitor C_i, respectively.

According to what was described above, the architecture in Fig. 2(a) can be changed to Fig. 4. Two types of delay in the clock generation path considered in this figure:

1. *Fixed delay* is made in order for the new decision requirements to be prepared by the control logic circuitry.
2. *Variable delay* that is designed for the D/A array capacitors settling.

3.2. Circuit Implementation

Fig. 5 shows the circuit implementation and the timing diagram of the proposed asynchronous clock generator. In the comparator clock generation, two types of delay has

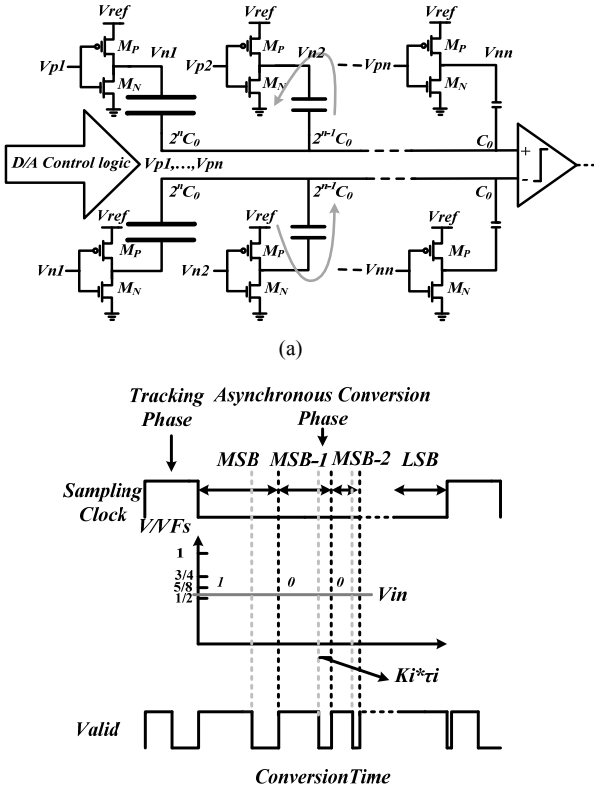


Fig. 3. (a) Schematics of the SAR ADC in asynchronous conversion phase (the cycle associated with generating the (MSB-1) bit). (b) Proposed asynchronous process approach.

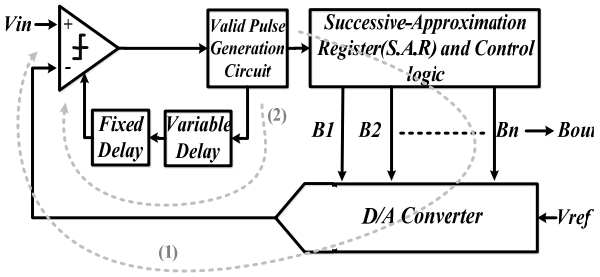


Fig. 4. Architecture of the proposed asynchronous SAR ADC.

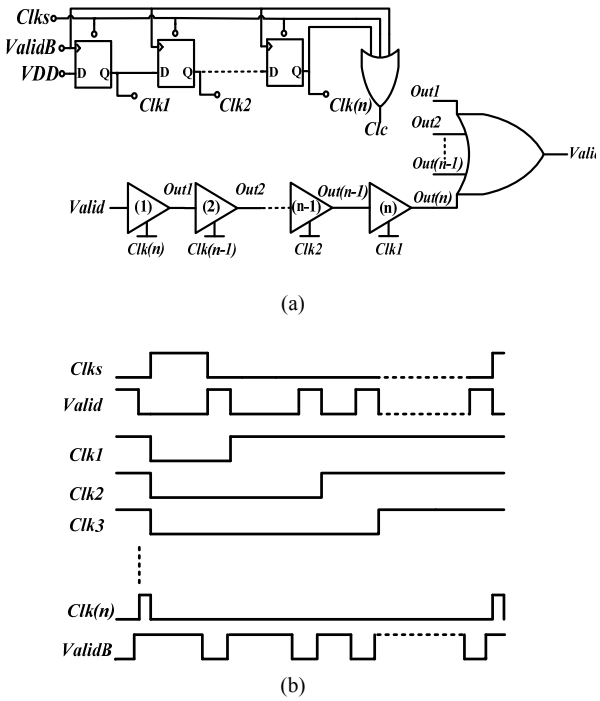


Fig. 5. (a) Proposed asynchronous clock generator circuit. (b) proposed asynchronous clock generator timing curves.

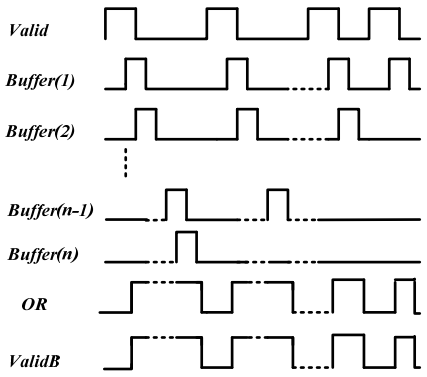


Fig. 6. Timing curves for buffers chain and OR gate circuits.

been considered [8], [9]. The first type (Fixed delay) due to the signal delay associated with the OR gate and the second (Variable delay) due to the internal delay associated with the buffer chain. (The buffer chain has a good accuracy because of utilizing the unary delay line.)

Each buffer includes two cascaded inverters with the same sizes and power supply voltages that make the same delay. A reset terminal is utilized for each buffer to eliminate its delay and reduce the power of the delay line that results in the reduction of the total power consumption of the ADC. Resetting the buffer makes the output logical zero. Therefore the input of the OR gate associated with this buffer output will be zero and the delay signal generated will be reduced. The reset signal required for the buffer line is made by the conventional asynchronous clock generator depicted in Fig. 5 and therefore does not need any more extra circuit.

The operation of the asynchronous clock generator circuit that, shown in Fig. 5, is as follows: at the comparison phase each buffer is active and its output becomes high' until the reset signal is applied. For example, the first buffer in the chain is the last one to be reset. Each buffer in the chain has a specific delay and the outputs of the buffers are connected to an n-input OR gate. Thus, resetting each buffer results in reduction in the delay signal (ValidB) generated by the OR gate. Fig. 6 shows the operation of the circuit.

In the case of an *n-bit* asynchronous SAR ADC with unary delays, 2^n buffers in the chain are required to produce the bits from MSB to LSB which drastically increase the size and power consumption of the clock generator circuit.

Moreover, when the D/A voltage changes, the switches in Fig. 3 (a) provide an overshoot due to C_{gd}. The D/A array

capacitors transfer the switch's overshoot to the D/A array capacitors output which increases the capacitive settling time. This is an important drawback at the nanometer technologies [10] and since the overshoot is the same for different capacitances [10], its effect is more on less significant bits. Thus, it is necessary not to dedicate very small settling time to the less significant bits capacitors of the D/A array compared with MSBs capacitors. Therefore, here, the number of buffers is set according to the number of the SAR ADC output bits and the total delay of the buffer chain can be designed based on the settling time of the MSB capacitor. In this way, with eliminating each buffer from the chain, the total delay of the chain is reduced for different D/A capacitor.

Recently, a binary delay line which is proportional to D/A array settling time has been published [8]. In this paper, the delay line has controlled with a separate circuits that consume extra power. Also for the overshoot effect and making the new decision no time has dedicated results some errors (i.e., metastability) in the comparator decision.

As it can be seen in the Fig. 6, the delay associated with the chain buffers is more than the pulse width dedicated to a single buffer and, thus, the outputs *Valid B* and *Valid* in Fig. 5 are not of the same phases.

If the output of the OR gate Set to 1, the clock of the comparator becomes zero and the comparator output valid data is sent to the control logic circuitry. In this method, without requiring the path with no delay, such as in [8], the comparator output valid data can be sent to the control logic circuitry and the comparator clock can be kept zero for the new decision and then the comparator's clock becomes 1.

3.3. Power Consumption and Conversion Time

In the conventional SAR ADC, the D/A array capacitors are charged or discharged in each decision phase through the on resistance of the switch (R_{on}). However, the time constant of the D/A array capacitors is determined based on the settling accuracy requirement of the largest D/A array capacitor (MSB capacitor). The period of each decision phase in the conventional asynchronous process is according to the following equation.

$$T_{Si} = T_{D/A} + T_0 + T_{Comp} \tag{1}$$

where T_0 is the specified time for the control logic to prepare its outputs (Fig. 4), and T_{Comp} is the specified period for the comparator to prepare its output. The conversion time in the conventional asynchronous process is as

$$T_S = T_{SW} + \sum_{i=1}^{n}(T_{Si}) = T_{SW} + n \times (T_0 + T_{Comp}) + \sum_{i=1}^{n} T_{D/A} = T_{SW} + T_{Fix} + \sum_{i=1}^{n}(T_{D/A}) \tag{2}$$

Here, T_{SW} is the sampling time of the bootstrap switches that is similar to the proposed asynchronous process and T_{Fix} is the time dedicated to the comparator decisions and the time required for the control logic circuitry in each conversion time. The period of each decision phase in the proposed asynchronous process is according to the following equation:

$$T'_{Si} = T_{D/A}\left(1 - \frac{i-1}{n}\right) + T_0 + T_{Comp} \quad i = 1,2,3,\dots,n \tag{3}$$

As seen, the D/A settling time is reduced form MSB ($i = 1$) to LSB ($i = n$) capacitors. The conversion time in the proposed asynchronous process is as follows:

$$T'_S = T_{SW} + \sum_{i=1}^{n}(T'_{Si}) = T_{SW} + \sum_{i=1}^{n}\left(T_{\frac{D}{A}}\left(1 - \frac{i-1}{n}\right) + T_0 + T_{Comp}\right) = T_{SW} + T_{Fix} + \sum_{i=1}^{n}\left(T_{\frac{D}{A}}\left(1 - \frac{i-1}{n}\right)\right) \tag{4}$$

According to (2) and (4):

$$\frac{T'_S}{T_S} = \frac{T_{SW} + T_{Fix} + \sum_{i=1}^{n}\left(T_{\frac{D}{A}}\left(1 - \frac{i-1}{n}\right)\right)}{T_{SW} + T_{Fix} + \sum_{i=1}^{n} T_{\frac{D}{A}}} < 1 \rightarrow \frac{f'_S}{f_S} > 1 \tag{5}$$

This shows the amount of the improvement in the sampling frequency of the proposed SAR ADC as compared to its conventional counterpart.

4. Design of a 10-bit 4-32 MS/s Asynchronous SAR ADC

The proposed asynchronous process has been applied to a 10-bit 4-32MS/s SAR ADC in a 130-nm digital CMOS technology. The converter schematic with two different supply levels is shown in Fig. 7. Two approaches are used to minimize the power consumption in this design:

1. Using a downward monotonic capacitor switching procedure (will be explained later) that decreases the average switching energy and the total D/A capacitance up to 81% and 51%, respectively [1].

The power consumption of the digital logic devices is proportional to the square of the power supply level [9]. Therefore, lower power supply (0.6 V) is applied to the control logic circuitry and the proposed asynchronous clock generator circuit, and higher power supply level (1.2 V) is applied to the other devices. According to the simulation results, the power consumption of the control logic circuitry and the proposed asynchronous clock generator circuit with lower supply (0.6 V) is about 1/3 of this value with higher supply (1.2 V).

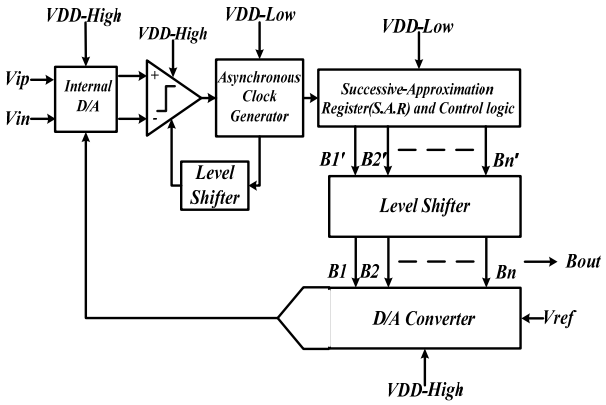


Fig. 7. SAR ADC schematics with two different supply levels.

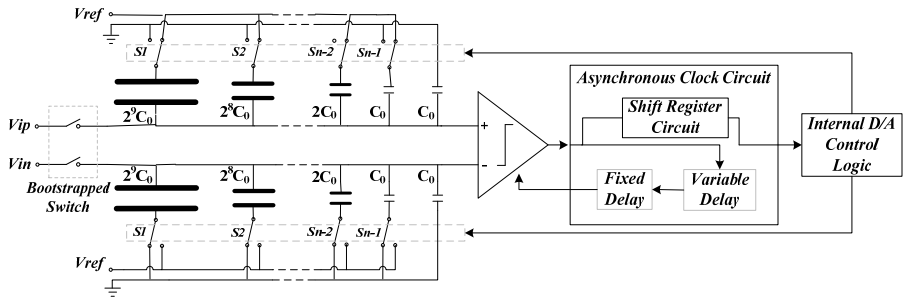
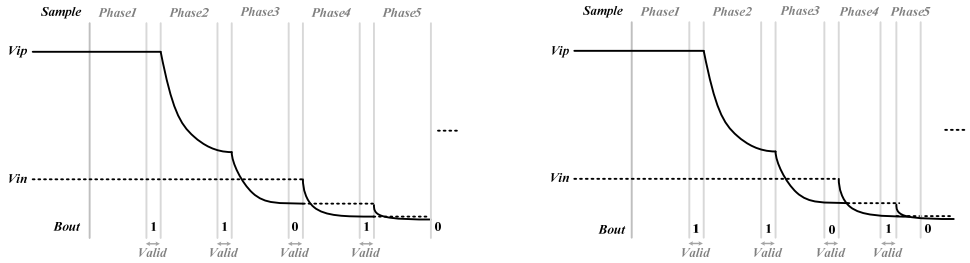


Fig. 8. Schematics of the 10-bit SAR ADC with a monotonic capacitor switching procedure and the proposed asynchronous clock generator circuit.



(a) (b)

Fig. 9. Transitions in the comparator inputs in (a) the conventional (b) the proposed monotonic capacitor switching procedure.

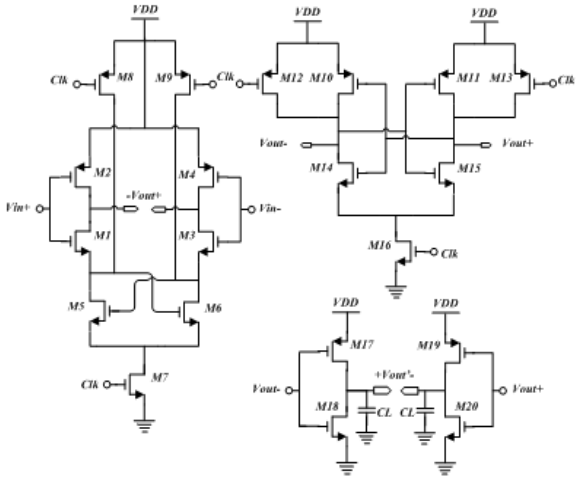


Fig. 10. Schematics of the dynamic comparator and CMOS inverters.

4.1. Monotonic Capacitor Switching Procedure

The schematics of the 10-bit SAR ADC with a monotonic capacitor switching procedure and the proposed asynchronous clock generator circuit are shown in Fig. 8. In this converter, in order to cancel the effect of the substrate, common mode and supply noise, differential structure has been used. The monotonic capacitor switching procedure can be upward or downward. In this design, in order to make the capacitive settling time of the D/A capacitive array through the NMOS transistors, the downward monotonic capacitor switching procedure has been used [1].

The converter functional steps are as follows: in the sampling phase, the bottom plates of all the D/A array capacitors are reset to V_{ref} and their top plates sample the input via two bootstrap switches that are used to increase the settling speed and the input bandwidth [1]. In the end of the sampling phase, the D/A capacitive array is disconnected from the input and with no switching, the MSB bit is compared with the D/A capacitive array voltage. Then, based on the comparator decision, the largest capacitor (MSB-1) in one of the two D/A sides (negative or positive) is selected and connected to the ground and the other capacitors remain unchanged [1]. In this way, in each comparison phase, only one capacitance is discharged to the ground from one of the two positive or negative D/A sides and, thus, the switching and the control circuitry power consumption is reduced, as compared to the conventional approach.

The transitions in the comparator inputs in the conventional and the proposed monotonic capacitor switching procedure are shown in Figs. 9(a) and 9(b), respectively.

4.2. Comparator

The comparator uses a completely dynamic structure that consists of two parts namely pre-amplifier and latch. Both parts operate in the same phase and the comparator can pull the latch and the pre-amplifier output nodes up to the power supply voltage level in the second phase. Offset cancellation can also be considered in the comparator [11], [12]. The circuit diagram in Fig. 10 has been used in simulations that has been obtained from [13] with adding M_2 and M_4. In this way, a dual rail pre-amplifier is then achieved that can work with a common mode near the ground that is necessary for the downward monotonic capacitor switching procedure in Fig. 8. Mismatch between the D/A array capacitors can be calibrated as reported in [14] and [15]. In order to reduce unit capacitor to ~ 1 fF [16], [17].

4.3. Level Shifter

Since there are two different power supply levels in the circuit, in order to convert the lower voltage level (0.6 V) to a higher one (1.2 V), the conventional level shifter shown in Fig. 11 is used [18]. The conventional level shifter takes up smaller area and consumes less power when its lower voltage level is 0.6 V.

4.4. Proposed Asynchronous Clock Generator Circuit

In this design, the proposed asynchronous clock generator circuit with a buffer chain with 10 buffers has been used that is shown in Fig. 12. In the monotonic capacitor switching procedure, nine stages are needed, but to notify a valid result in the converter output, a new delay unit is also added. Thus, the proposed asynchronous clock generator circuit in Fig. 12 has been designed with 10 buffers.

5. Simulation Results

In Fig. 13, comparison of the power dissipation and conversion time between conventional and proposed 10-bit 4-MS/s SAR ADC with a monotonic capacitor switching procedure has been shown. In this figure, the difference in the dedicated pulse width to the D/A capacitive array between the conventional and the proposed asynchronous process has been investigated.

In this simulation, all of the SAR ADC conditions are the same in the two structures but in the conventional one, none of the chain buffers are reset, unlike the proposed one and, thus both the power dissipation and the conversion time are more compared to the proposed one that is according to the equation (6).

The ADC total power consumption division is shown in Fig. 14 and the density of the power spectrum of the converter output versus frequency is shown in Fig. 15.

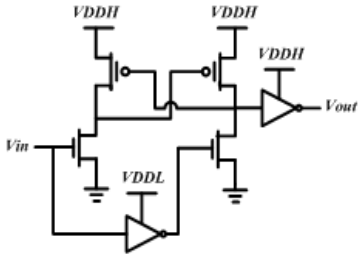


Fig. 11. Schematics of the conventional level shifter circuit.

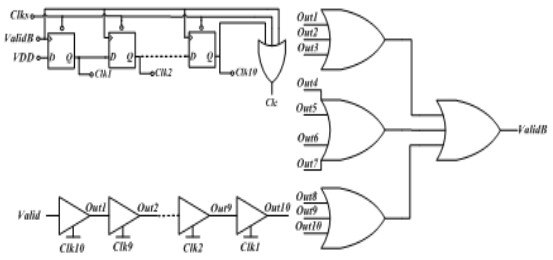
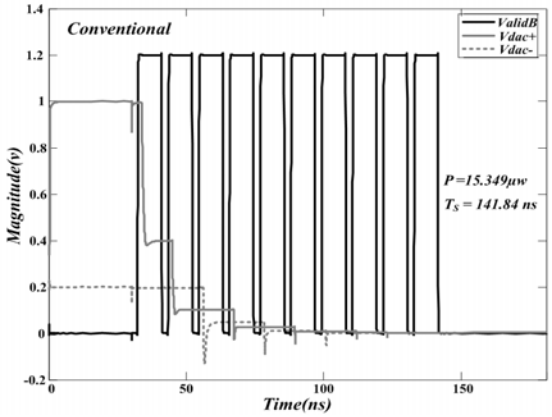


Fig. 12. Schematics of the proposed asynchronous clock generator circuit with 10 delay units for a 10-bit asynchronous SAR ADC.

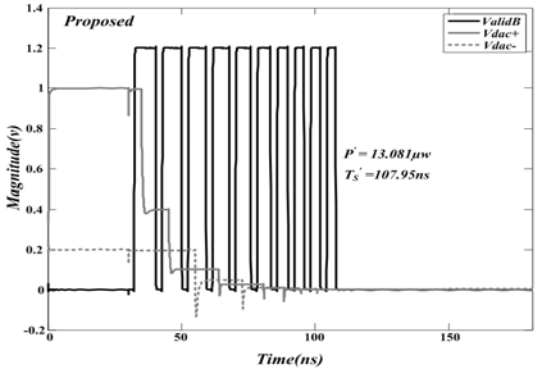
In this figure, VDD-high is the higher supply level (that is 1.2V) and has the highest power dissipation and VDD-low is the lower supply level (that is 0.6V) and has a lower power dissipation.

In Fig. 16, the parameters ENOB, FOM, and power consumption versus input frequency is shown.

The simulations results of the 10-bit 4-MS/s SAR ADC for the different process and temperature corners are shown in Table 1. Table 2 shows the specification summary versus sampling frequency. Table 3 presents a comparison to state-of-the-art works between the proposed paper results and some other papers.



(a)



(b)

Fig. 13. Comparision of the conversion time and power dissipation between (a) Conventional (b) Proposed 10-bit 4-MS/s SAR ADC with a monotonic capacitor switching procedure.

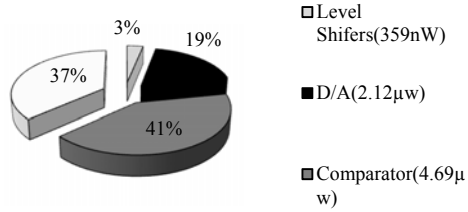


Fig. 14. ADC total power consumption division approach in its different devices at F_S=4MS/s, $f_{in}=\frac{31}{128}F_S$.

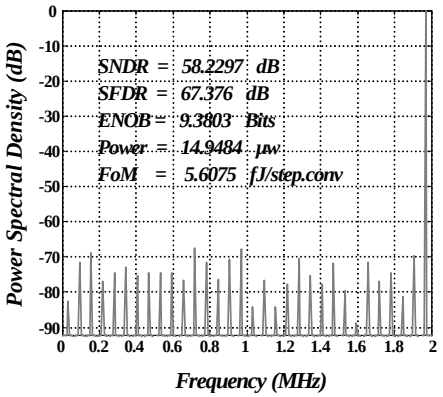


Fig. 15. Simulated 2,048-point FFT spectrum at 4-MS/s.

Table 1. Simulated Dynamic Performance at Different Corners

Corners	SFDR (dBc)	ENOB (bit)	Power (µw)	FOM (fJ/c-s)
T.T@27°C	69.365	9.348	13.758	5.277
T.T@37°C	66.838	9.353	13.794	5.271
F.F@27°C	65.277	9.192	15.622	6.676
F.F@0°C	66.868	9.403	14.618	5.398
S.S@27°C	66.528	9.357	13.900	5.301
S.S@100°C	61.052	8.4502	13.8684	9.9132

Table 2. Specification Summary Versus Sampling Frequency

Sampling Frequency (MS/s)	4	8	16	32
ENOB(Bits)	9.35	9.38	9.41	9.28
Power(µw)	13.76	31.17	59.74	185.80
FoM(fJ/c-s)	5.28	5.86	5.50	9.35
V_{DDL} (v)	0.6	0.6	0.75	1.2
V_{DDH} (v)	1.2	1.2	1.2	1.2

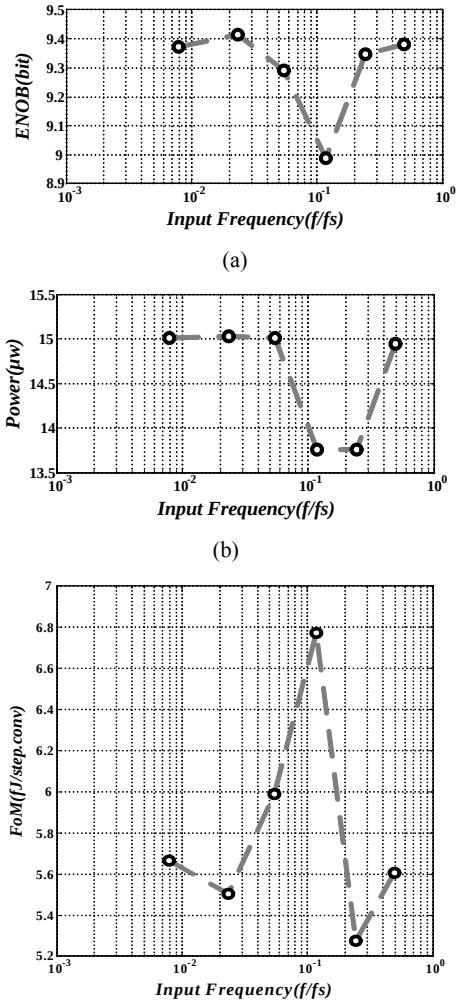


Fig. 16. The parameters (a) ENOB (b) FOM (c) Power dissipation of the SAR ADC versus input frequency at 4-MS/s.

Table 3. Comparison to State-of-the-Art Works

Specifications	[1]	[8]	[17]	[19]	[20]	[21]	[22]	This Work
Technology(nm)	130	40	90	130	90	40	130	130
Supply Voltage(V)	1.2	0.6&0.7	1.1	1.2	0.7	0.5	0.4&1	0.6&1.2
Sampling Rate(MS/s)	50	8.2	4	64	4	1.1	0.001	4
Resolution(Bits)	10	10	10	10	10	8	10	10
DAC unit Capacitor(fF)	4.8	0.5	0.6	5.5	5	0.5	13.5	1
ENOB(Bits)	9.2	7.7	9	8	9	7.5	9.1	9.35
Power(µw)	826	21.5	17.4	1325	11	1.2	0.053	13.76
FOM(fJ/c-s)	29	12.5	8.5	78.7	5.2	6.3	94.5	5.3
Type	measurement	measurement	measurement	measurement	measurement	measurement	measurement	Simulation

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